WHAT IS CLAIMED, IS:

1. Method for pre-processing input signals of interfaces of
   different type for common-format central processing, us-
   ing a common system clock, said different interface types
   being associated with differing sample clock frequencies
   and/or differing data frame or data word formats, said
   method including the steps:
   - generating from the different-type interface input sig-
     nals system clock synchronised input signals;
   - channel decoding said system clock synchronised input
     signals according to the differing channel protocols re-
     lated to said different-type interfaces, thereby provid-
     ing corresponding PCM bitstream format signals having a
     uniform word format;
   - further processing said PCM bitstream format signals so
     as to form therefrom sample words that are stored in an
     intermediate store, e.g. a FIFO, from which the sample
     words are fed to said central processing.

2. Method for pre-processing output signals for interfaces
   of different type in a common-format central processing
   using a common system clock, said different interface
   types being associated with differing sample clock fre-
   quencies and/or differing data frame or data word for-
   mats, said method including the steps:
   - further processing sample words that were output from
     said central processing and stored in an intermediate
     store, e.g. a FIFO, by forming system clock synchronised
     PCM bitstream format signals therefrom, which PCM bit-
     stream format signals have a uniform word format and are
     related to said interfaces of different type;
   - channel encoding said system clock synchronised PCM bit-
     stream format signals having a uniform word format ac-
     cording to the differing channel protocols related to
     said different-type interfaces, thereby providing corre-

sponding system clock synchronised output signals;
- generating from said system clock synchronised output
  signals interface-type related output signals (SADO) that
  are no more system clock synchronised but conform to said

5   type of interface.

3. Apparatus for pre-processing input signals of interfaces
   of different type for common-format central processing,
   using a common system clock, said different interface

10   types being associated with differing sample clock fre-
   quencies and/or differing data frame or data word for-
   mats, said apparatus including:
- means for generating from the different-type interface
  input signals system clock synchronised input signals;

15   - means for channel decoding said system clock synchronised
   input signals according to the differing channel proto-
   cols related to said different-type interfaces, thereby
   providing corresponding PCM bitstream format signals hav-
   ing a uniform word format;

20   - means for further processing said PCM bitstream format
   signals so as to form therefrom sample words that are
   stored in an intermediate store, e.g. a FIFO, from which
   the sample words are fed to a central processing.

25   4. Apparatus for pre-processing output signals for inter-
   faces of different type in a common-format central proc-
   essing using a common system clock, said different inter-
   face types being associated with differing sample clock
   frequencies and/or differing data frame or data word for-

30   mats, said apparatus including:
- means for further processing sample words that were out-
  put from said central processing and stored in an inter-
  mediate store, e.g. a FIFO, by forming system clock syn-
  chronised PCM bitstream format signals therefrom, which

35   PCM bitstream format signals have a uniform word format
   and are related to said interfaces of different type;

- means for channel encoding said system clock synchronised
  PCM bitstream format signals having a uniform word format
  according to the differing channel protocols related to
  said different-type interfaces, thereby providing corre-
5 sponding system clock synchronised output signals;
- means for generating from said system clock synchronised
  output signals interface-type related output signals that
  are no more system clock synchronised but conform to said
  type of interface.
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5. Method according to claim 1 or 2, wherein said interface
   types include at least two of IEC958, I2S, AC-Link and
   ADAT.

15 6. Method according to claim 1 or 2, wherein some individual
    samples are marked or checked with their channel type in
    the system clock synchronised processing in order to de-
    tect and avoid channel permutation, said channel permuta-
    tion occurring e.g. in case of insertion or deletion of
20   samples, said marking being carried out e.g. by using
    subcode bits that are otherwise not used in said system
    clock synchronised processing.

7. Method according to claim 1 or 2, wherein for DMA data
25   block transfer in connection with said intermediate stor-
    age an LF marking is carried out for the first word of·
    each DMA data block and is evaluated in order to reduce
    the number of processor operations when preparing a DMA
    buffer output.
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8. Method according to claim 1 or 2, wherein for facilitat-
   ing a precisely timed start-up of a stream unit that per-
   forms said further processing of the sample words, an in-
   ternally generated time stamp is supplied to the stream
35   unit by the central processing.

9. Method according to one of claims 1 to 8, wherein for synchronisation of interface signals that have separate clock and data or sync signals to said system clock, two succeeding D flip-flops are used that are clocked by the same edge of the clock to be synchronised.

5. Apparatus according to claim 3 or 4, wherein said interface types include at least two of IEC958, I2S, AC-Link and ADAT.

6. Apparatus according to claim 3 or 4, wherein some individual samples are marked or checked with their channel type in the system clock synchronised processing in order to detect and avoid channel permutation, said channel permutation occurring e.g. in case of insertion or deletion of samples, said marking being carried out e.g. by using subcode bits that are otherwise not used in said system clock synchronised processing.

7. Apparatus according to claim 3 or 4, wherein for DMA data block transfer in connection with said intermediate storage an LF marking is carried out for the first word of each DMA data block and is evaluated in order to reduce the number of processor operations when preparing a DMA buffer output.

8. Apparatus according to claim 3 or 4, wherein for facilitating a precisely timed start-up of a stream unit that performs said further processing of the sample words, an internally generated time stamp is supplied to the stream unit by the central processing.

9. Apparatus according to claim 3 or 4, wherein for synchronisation of interface signals that have separate clock and data or sync signals to said system clock, two succeeding D flip-flops are used that are clocked by the

same edge of the clock to be synchronised.